WHAT IS CLAIMED IS:

1. A fin field effect transistor, comprising:

a fin comprising a channel;

a source region formed adjacent a first end of the fin;

a drain region formed adjacent a second end of the fin;

a first layer of metal material comprising a first gate electrode, wherein the first layer of metal material is formed adjacent the fin; and

a second layer of metal material formed adjacent the first layer, the second layer of metal material comprising a second gate electrode, wherein the first layer of metal material comprises a different work function than the second layer of metal material, wherein the second layer of metal material is selectively diffused into the first layer of metal material via metal interdiffusion.

2. The transistor of claim 1, wherein the first layer of metal material comprises Ti or Ni.

3. The transistor of claim 2, wherein the second layer of metal material comprises Ni or Ti.

4. The transistor of claim 1, further comprising:

a gate insulation layer formed between the fin and the first layer of metal material.

5. The transistor of claim 4, wherein the gate insulation layer comprises at least one of SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_3, HFSiO(x) ZnS, and MgF_2.

6. The transistor of claim 1, wherein the first layer of metal material has a thickness ranging from about 300Å to about 1000Å.

7. The transistor of claim 6, wherein the second layer of metal material has a width ranging from about 300Å to about 1000Å.

8. A method of forming a multiple voltage threshold fin field effect transistor (FinFET), comprising:

forming a fin;

forming a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin;

forming a dummy gate comprising a first material in a first pattern over the fin;

forming a dielectric layer adjacent sides of the dummy gate;

removing the first material to form a trench in the dielectric layer corresponding to the first pattern;

forming a first metal gate layer in the trench, wherein the first metal gate layer comprises a first metal material; and

forming a second metal gate layer in the trench adjacent the first metal gate layer, wherein the second metal gate layer comprises a second metal material and wherein the second metal material selectively diffuses through the first metal material via metal interdiffusion to produce a multiple voltage threshold FinFET.

9. The method of claim 8, wherein the dielectric layer comprises tetraethylorthosilicate.

10. The method of claim 8, further comprising:

forming a gate insulation layer in the trench prior to forming the first metal gate layer.

11. The method of claim 10, wherein the gate insulation layer comprises at least one of SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_3, HFSiO(x) ZnS, and MgF_2.

12. The method of claim 8, wherein forming the dummy gate comprises:

depositing a layer of polysilicon over the fin; and

etching the polysilicon layer to form the dummy gate in the first pattern.

13. The method of claim 8, wherein forming the first metal gate layer comprises:

depositing the first metal material in the trench to a thickness ranging from about 300Å to about 1000Å.

14. The method of claim 13, wherein forming the second metal gate layer comprises:

depositing the second metal material adjacent the first metal material in the trench to a thickness ranging from about 300Å to about 1000Å.

15. A method of forming a fin field effect transistor comprising a fin and a source region adjacent a first end of the fin and a drain region adjacent a second end of the fin, the method comprising:

forming a dummy oxide layer over the fin;

depositing a layer of first material over the fin and dummy oxide layer;

etching the layer of the first material to form a dummy gate in a first pattern;

depositing a dielectric layer over the dummy gate and source and drain regions;

planarizing the dielectric layer to expose a top surface of the dummy gate;

removing the first material to form a trench in the dielectric layer corresponding to the first pattern;

forming a gate insulation layer in the trench;

forming a first gate layer in the trench, the first gate layer comprising a first metal material, wherein the first metal material comprises a first work function; and

forming a second gate layer in the trench, the second gate layer comprising a second metal material, wherein the second metal material comprises a second work function.

16. The method of claim 15, wherein the first work function is different than the second work function.

17. The method of claim 15, wherein forming the first gate layer comprises:

depositing the first metal material in the trench to a thickness ranging from about 300Å to about 1000Å, and wherein forming the second gate layer comprises:

depositing the second metal material adjacent the first metal material in the trench to a thickness ranging from about 300Å to about 1000Å.

18. The method of claim 15, wherein the first material comprises polysilicon.

19. The method of claim 15, wherein the gate insulation layer comprises at least one of SiO, SiO_2, SiN, SiON, HFO_2, ZrO_2, Al_2O_3, HFSiO(x) ZnS, and MgF_2.